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[Title of the Invention]

METHOD OF DRIVING ANTIFERROELECTRIC LIQUID CRYSTAL DISPLAY DEVICE

[Abstract]

[Object] To provide a method of driving an antiferroelectric liquid crystal display device to perform high-speed high-contrast display while reducing image burn-in.

[Solving Means] In a resetting period, the potential difference between antiferroelectric liquid crystal cells is set to 0 V and scanning electrodes and signal electrodes are short-circuited to ground, thereby removing residual charge components in the cells and a drive circuit to reduce image burn-in due to variation in the amount of charge.

[Scope of Claims]

[Claim 1] A method of driving an antiferroelectric liquid crystal in an antiferroelectric liquid crystal display device in which the antiferroelectric liquid crystal is sandwiched between a pair of substrates respectively having on their opposed surfaces a plurality of scanning electrodes and a plurality of signal electrodes, and which have pixels in a matrix array,

wherein said antiferroelectric liquid crystal has three states: a first ferroelectric state, a second ferroelectric state in which a ferroelectricity is exhibited when a voltage having a polarity opposite from that of the first ferroelectric state is applied, and an antiferroelectric state,

wherein one period for writing to each pixel comprises at least one scanning period, said scanning period including a selecting period in which a selecting pulse for determining the amount of light transmitted through the pixel is applied, a resetting period in which a resetting pulse for setting the antiferroelectric liquid crystal in a certain condition before the selecting period is applied, and a non-selecting period in which the amount of transmitted light determined in the selecting period is maintained, and

wherein both the scanning electrodes and the signal electrodes are short-circuited to ground in said resetting period.

[Claim 2] The method of driving an antiferroelectric liquid crystal display device according to claim 1, wherein voltage waveforms in successive two scanning periods are symmetrical about 0 V.

[Detailed Description of the Invention]

[0001]

[Technical Field to which the Invention belongs]

The present invention relates to a method of driving an antiferroelectric liquid crystal display device having a liquid crystal layer formed of an antiferroelectric liquid crystal, such as a liquid crystal display panel having pixels in a matrix

array or a liquid crystal light shutter array.

[0002]

[Prior Art]

In Japanese Patent Application Laid-Open No. Hei 2-173724 of the invention by Nippon Denso Co., Ltd. and Showa Shell Sekiyu K.K., it was disclosed that liquid crystal panels using an antiferroelectric liquid crystal have a wide viewing angle, are capable of high-speed response, have favorable multiplexing characteristics, etc.. Since then, studies about liquids crystal panels using an antiferroelectric liquid crystal have been made energetically.

[0003]

Fig. 2 is a diagram of the configuration of a liquid crystal cell showing the placement of polarizing plates in a case where an antiferroelectric liquid crystal is used in a display. A liquid crystal cell 22 is placed between polarizing plates 21 in a cross-nicol relationship so that the optic axis of molecules when no electric field is applied is substantially parallel to the polarization axis of one of the polarizing plates, thereby enabling display in black when no electric field voltage is applied and display in white when an electric field is applied. When a voltage applied to the liquid crystal cell of the above-described cell configuration is changed, changes in transmittance are plotted in a graph to depict loops such as those shown in Fig. 3. A voltage value at which the transmittance starts changing when the voltage applied is increased is represented by V1; a voltage value at which the change in transmittance is saturated is represented by V2; a voltage value at which the transmittance starts decreasing when the voltage value is reduced is represented by V5; a voltage value at which transmittance starts changing when the voltage of the opposite polarity is applied and when the absolute value thereof is increased is represented by V3; a voltage value at which the change in transmittance is saturated is represented by V4; and a voltage value at which the transmittance starts decreasing when contrarily the absolute value of the voltage

is reduced is represented by V6. As can be understood from Fig. 3, a first ferroelectric state is selected when the voltage value becomes equal to or higher than a threshold value of antiferroelectric liquid crystal molecules; a second ferroelectric state is selected according to the different polarity of the applied voltage; and an antiferroelectric state is selected from one of these ferroelectric states when the voltage value becomes smaller than a threshold value.

[0004]

As shown in Fig. 4, in the conventional drive method, the first or second ferroelectric state or the antiferroelectric state is selected in a selecting period (Se), and the corresponding state is maintained during a subsequent non-selecting period (NSe). That is, the amount of transmitted light set by a selecting pulse in the selecting period (Se) is maintained during the subsequent non-selecting period (NSe) to perform display.

[0005]

If the state of molecules of the antiferroelectric liquid crystal immediately before the application of a selecting pulse in each selecting period is not constant, it is difficult to correctly set the amount of light transmitted through a pixel to a predetermined value. A method has therefore been practiced in which resetting each pixel to the antiferroelectric state is always performed regardless of the preceding state of the pixel. This method for resetting to the antiferroelectric state is, for example, a method of setting the voltage value to 0 V in a resetting period to enable resetting to the antiferroelectric state by natural relaxation of the antiferroelectric liquid crystal depending on properties, such as viscosity, resiliency, etc., of the antiferroelectric liquid crystal itself, or a method of applying a suitable voltage of the opposite polarity to effect resetting to the antiferroelectric state.

[0006]

[Problems to be solved by the Invention]

The former resetting method based on natural relaxation of antiferroelectric liquid crystal molecules from the ferroelectric state ensures reliable resetting to the antiferroelectric state, but it is disadvantageous in that, if the state of one pixel immediately before the resetting period is the first or the second ferroelectric state, a considerably long time is required to reset the pixel to such an initialized state that the charge across the liquid crystal layer accumulated by the preceding writing is completely eliminated, resulting in retardation of frame writing. In the latter method of applying a suitable voltage to effect resetting to the antiferroelectric state, a voltage of the - (minus) polarity is applied if the state immediately before the resetting period is the first ferroelectric state, and a voltage of the + (plus) polarity is applied if the state immediately before the resetting period is the second ferroelectric state. Also in this method, voltages are always applied across the liquid crystal layer, so that excess charge exists. Thus, the resetting performance according to the conventional methods for setting to the antiferroelectric state is affected by the preceding display state since there is no discharge route, resulting in image burn-in in the screen.

[0007]

As a technique similar to the method for resetting to the antiferroelectric state, a method of temporarily setting the antiferroelectric liquid crystal in the ferroelectric state at the time of writing is disclosed in Japanese Patent Application Laid-open No. Hei 5-100208.

[0008]

In an embodiment described in Japanese Patent Application Laid-open No. Hei 5-100208, the response (rising speed) of a liquid crystal is improved by application of a voltage high enough to effect a change to the ferroelectric state before application of a gray-scale voltage. The method disclosed in Japanese Patent Application Laid-open No. Hei 5-100208, however, is intended to reduce the time required to set the

antiferroelectric liquid crystal in the ferroelectric state, and no mention is made of drive for change to the antiferroelectric state in that document.

[0009]

The present invention has been made to solve the above-mentioned problems, and has an object to provide a method of driving an antiferroelectric liquid crystal display device which reduces image burn-in resulting from the difference between the amounts of charges of residual charge components in cells and a drive circuit to perform high-speed high-contrast display.

[0010]

[Means for solving the Problems]

To attain the above-mentioned object of the present invention, a method of driving an antiferroelectric liquid crystal display device according to the present invention employs the following means.

[0011]

In an antiferroelectric liquid crystal display device in which an antiferroelectric liquid crystal is sandwiched between a pair of substrates respectively having on their opposed surfaces a plurality of scanning electrodes and a plurality of signal electrodes, and which have pixels in a matrix array, the antiferroelectric liquid crystal has three states: a first ferroelectric state, a second ferroelectric state in which a ferroelectricity is exhibited when a voltage having a polarity opposite from that of the first ferroelectric state is applied, and an antiferroelectric state. Also in this pixel, one period for writing to each pixel comprises at least one scanning period, and the scanning period includes a selecting period in which a selecting pulse for determining the amount of light transmitted through the pixel is applied, a resetting period in which a resetting pulse for setting the antiferroelectric liquid crystal molecules in a certain condition before the selecting period is applied, and a non-selecting period in which the amount of transmitted light determined in the selecting

period is maintained. Specifically, both the scanning electrodes and the signal electrodes are short-circuited to ground in the resetting period.

[0012]

Also, voltage waveforms applied to the pixel in successive two scanning periods are formed so as to be symmetrical about 0 V, thus forming an alternating-current form.

[0013]

(Function)

The antiferroelectric liquid crystal is set in the first or second ferroelectric state when the absolute value of the applied voltage is equal to or higher than a threshold value, as shown in Fig. 3. At this time, if the cell configuration is such as shown in Fig. 2, antiferroelectric liquid crystal molecules are always set in the antiferroelectric state during the resetting period according to the drive method of the present invention. To do so, in the resetting period, the threshold voltage necessary for switching the antiferroelectric liquid crystal molecules from the first or second ferroelectric state to the antiferroelectric state is applied. Ordinarily, this voltage value is smaller than the voltage value necessary for switching from the first or second ferroelectric state to the second or first ferroelectric state. This voltage value is set to 0 V, and simultaneously, both the scanning electrodes and the signal electrodes are short-circuited to ground, thereby removing residual charge components between the liquid crystal cells and in the drive circuit. This method eliminates the need for the voltage required in the conventional method for resetting to the antiferroelectric state. Also, this method enables resetting at a markedly high speed in comparison with the method of resetting to the antiferroelectric state by natural relaxation based on the essential properties of the liquid crystal.

[0014]

In the drive method according to the present invention,

the state of the antiferroelectric liquid crystal is reset to the antiferroelectric state and residual charge components in the liquid crystal cells and the drive circuit are simultaneously removed each time writing is performed, thus stabilizing display with respect to each writing period. Since the antiferroelectric liquid crystal can be set in the antiferroelectric state by applying a voltage of 0 V in the resetting period, there is no need for a resetting pulse impressed voltage. The display state (the state of the antiferroelectric liquid crystal) is determined in a short selecting period. It is therefore possible to perform high-speed display by changing the state of the liquid crystal between the ferroelectric state and the antiferroelectric state, thereby reducing image burn-in due to residual charge components. The present invention has been achieved by focusing attention to this point. The present invention will be described below with respect to an embodiment mode thereof.

[0015]

[Embodiment Mode of the Invention]

An embodiment mode of the present invention will be described in detail with reference to the drawings. Fig. 5 is a diagram showing the construction of a liquid crystal panel used in this embodiment mode. The liquid crystal panel used in this embodiment mode is constituted by a pair of glass substrates 53a and 53b having an antiferroelectric liquid crystal layer 56 having a thickness of about 2 im. Electrodes 54a and 54b are formed on opposed surfaces of the glass substrates, and high-polymer alignment films 55a and 55b are formed by application of the material over the electrodes. The high-polymer alignment films 55a and 55b are processed by rubbing. A first polarizing plate 51a is placed on the outer surface of one of the glass substrates so that the polarization axis of the polarizing plate and the rubbing axis are parallel to each other. A second polarizing plate 51b is placed on the outer surface of the other glass substrate so that its polarization axis forms an angle of 90° with the polarization

axis of the first polarizing plate 51a.

[0016]

Fig. 6 is a diagram showing the arrangement of scanning electrodes and signal electrodes. The scanning electrodes are indicated by X1, X2, and Xn, respectively, and signals electrodes are indicated by Y1, Y2, and Ym, respectively. The number of scanning electrodes is 480, and the number of signal electrodes is 640. Intersections of the scanning and signal lines shown by oblique lines correspond to pixels (A11, Anm).

[0017]

Fig. 1 is a diagram showing scanning voltage waveforms at the scanning electrode (Xn), signal voltage waveforms at the signal electrode (Ym), resultant voltage waveforms at the pixel (Anm) corresponding to the intersection of the scanning and signal electrodes, and resulting changes in transmittance, with respect to white display (ON(W)) and black display (OFF(B)) according to this embodiment mode of the present invention. In the drive waveforms used according to the present invention, a resetting time (Rs) was set as one phase and a selecting period (Se) was set as one phase. The one-phase pulse width was set to 50 is, and one writing period was formed by two scanning periods (SC1, SC2). The length of a non-selecting period (NSe) was about 45 ms. With respect to the scanning electrode (Xn) waveform, a holding voltage of 4 V was applied during the non-selecting period (NSe). This polarity was set with the same polarity as a voltage applied during the resetting period (Rs).

[0018]

The maximum absolute value of the crest value of a pulse applied during a scanning electrode (Xn) selecting period (Ss) was set to 20 V, and the maximum absolute value of a voltage applied to the signal electrode (Ym) was set to 4 V. To perform black display (OFF(B)), 0 V (resetting pulse) was applied through one phase in the resultant voltage waveform (Anm) in the first scanning period (SC1). The antiferroelectric liquid crystal then exhibited antiferroelectricity, and the amount of transmitted light was close to 0% in the resetting period.

However, in the subsequent selecting period (Se), a voltage of + 24 V (selecting pulse) in the resultant voltage waveform is applied through one phase. The antiferroelectric liquid crystal is thereby set in the first or second ferroelectric state, so that the amount of transmitted light becomes 100%, thus performing white display ON(W). In the non-selecting period (NSe), the ferroelectric liquid crystal is maintained in the antiferroelectric state. The resetting period is sufficiently shorter than the time period necessary for visual recognition by the observer. Therefore, the display can be visually recognized as white.

[0019]

In the case of black display OFF(B), 0 V (resetting pulse) is similarly applied through one phase in the resultant voltage waveform in the resetting period (Rs). The antiferroelectric liquid crystal exhibits an antiferroelectric state, and the amount of transmitted light is close to 0% in the resetting period. In the subsequent selecting period (Se), a voltage of + 16 V (selecting pulse) in the resultant voltage waveform is applied through one phase. Therefore, the antiferroelectric liquid crystal is not set in the first or second ferroelectric state, the antiferroelectric state is selected, and the amount of transmitted light is close to 0%, thus performing black display OFF(B). In the non-selecting period (NSe), the antiferroelectric liquid crystal is maintained in the antiferroelectric state, similar to the resetting period. The resetting period is sufficiently shorter than the time period necessary for visual recognition by the observer. Therefore, the display can be visually recognized as black.

[0020]

Two scanning periods (SC1, SC2) were set in one writing period, and the polarities of the voltage waveforms during these scanning periods were made symmetrical about 0 V to obtain an ac-current form.

[0021]

The result of use of the above-described method was that

the time required to reset the antiferroelectric liquid crystal to the antiferroelectric state was reduced although the applied resetting pulse voltage was 0 V. Also, with respect to any display in black or white, the period of time required as a selecting period was reduced and the desired display of any picture was performed at a high speed.

[0022]

This embodiment mode has been described with respect to the case of driving using a plurality of scanning electrodes and a plurality of signal electrodes. However, even in the case of driving with active elements, e.g., switching elements for forming pixels, the same effect can also be achieved as long as the voltage waveform applied to the pixel is a resultant voltage waveform corresponding to that in this embodiment mode.

[0023]

As described above with respect to the embodiment mode, the drive method of the present invention is used in such a manner that the liquid crystal cells and the drive circuit are short-circuited to ground during the resetting period to reset the antiferroelectric liquid crystal to the antiferroelectric state, residual charge components in the first or second ferroelectric state are also removed, and the drive circuit is further discharged, thereby always enabling signals to be newly written to the liquid crystal cells in the initialized state. Therefore, it is possible to reduce image burn-in during continuous driving. Further, since the resetting period is reduced, improved high-contrast display can be performed at a high speed.

[Brief Description of the Drawings]

[Fig. 1]

A diagram showing drive waveforms and resulting amounts of transmitted light in an antiferroelectric liquid crystal pixel in an embodiment mode of the present invention.

[Fig. 2]

A diagram showing the configuration of an antiferroelectric liquid crystal cell and polarizing plates in

the embodiment mode of the present invention.

[Fig. 3]

A diagram showing hysteresis curves of an antiferroelectric liquid crystal pixel in the embodiment mode of the present invention.

[Fig. 4]

A diagram showing a method of driving an antiferroelectric liquid crystal pixel in the conventional art.

[Fig. 5]

A diagram showing the construction of an antiferroelectric liquid crystal panel in the embodiment mode of the present invention.

[Fig. 6]

A diagram of the arrangement of scanning electrodes and signal electrodes in the embodiment mode of the present invention.

[Description of Symbols]

OFF(B)	black display
ON(W)	white display
SC1	first scanning period
SC2	second scanning period
Rs	resetting period
Se	selecting period
NSe	non-selecting period
Xn	scanning electrode
Ym	signal electrode
Anm	pixel
T	amount of transmitted light
21a, 21b	polarizing plates
22	liquid crystal cell
51a, 51b	polarizing plates
52a, 52b	sealing members
53a, 53b	glass substrates
54a, 54b	electrodes
55a, 55b	high-polymer alignment films

56	antiferroelectric liquid crystal
X1 to X480	scanning electrodes
Y1 to Y640	signal electrodes
A11, Anm	pixels

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Antiferroelectric liquid crystal driving method for liquid crystal display panel - involves short circuiting scanning and signal electrodes with ground during reset period

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Patent Family:

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Abstract (Basic): JP 11231286 A

NOVELTY - Antiferroelectric liquid crystal exhibits two ferroelectric states and a dielectric state based on the voltage applied to the liquid crystal. Pixel write-in operation is performed during the scanning period. Scanning and signal electrodes are short circuited with the ground during the reset period (RS). DETAILED DESCRIPTION - Reset pulse for setting the liquid crystal to a fixed state is applied during the reset period before the selection period (Se). Selection pulse for determining the permeable quantity of light of the pixel is applied during the selection period. Permeable quantity of light determined during the selection period is held during the non-selection period (NSe).

USE - For liquid crystal display panel and liquid crystal optical shutter array.

ADVANTAGE - Eliminates generation of braking phenomenon due to continuous driving of liquid crystal, by shortening reset period.

DESCRIPTION OF DRAWING(S) - The figure shows the drive wave form of the antiferroelectric liquid crystal display element. (NSe) Non-selection period; (RS) Reset period; (Se) Selection period.

Dwg. 1/6

Title Terms: LIQUID; CRYSTAL; DRIVE; METHOD; LIQUID; CRYSTAL; DISPLAY; PANEL; SHORT; CIRCUIT; SCAN; SIGNAL; ELECTRODE; GROUND; RESET; PERIOD
Derwent Class: P81; P85; U14
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International Patent Class (Additional): G09G-003/36
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DRIVING METHOD FOR ANTIFERROELECTRIC LIQUID CRYSTAL DISPLAY ELEMENT

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ABSTRACT

PROBLEM TO BE SOLVED: To enable high-speed and high-contrast display by reducing a burning phenomenon caused by a difference in the electric charge amount of a residual electric charge component between cells and at a driving circuit by short- circuiting the interval of liquid crystal cells and the driving circuit with a ground during a reset period.

SOLUTION: A liquid crystal panel is composed of a pair of glass substrates 53a and 53b having antiferroelectric liquid crystal layers 56. During the reset period, an antiferrodielectric liquid crystal molecule is turned into antiferroelectric state. Therefore, a threshold voltage required for switching the antiferrodielectric liquid crystal molecule from first or second ferroelectric state to antiferroelectric state is impressed during the reset period. Ordinarily, this voltage value is lower than a voltage value required for switching from the first or second ferrielectric state to the second or first ferroelectric state. By turning this voltage value to 0 V and simultaneously short-circuitting both scanning side and signal side electrodes with the ground, the residual electric charge component between the liquid crystal cells and at the driving circuit is removed.

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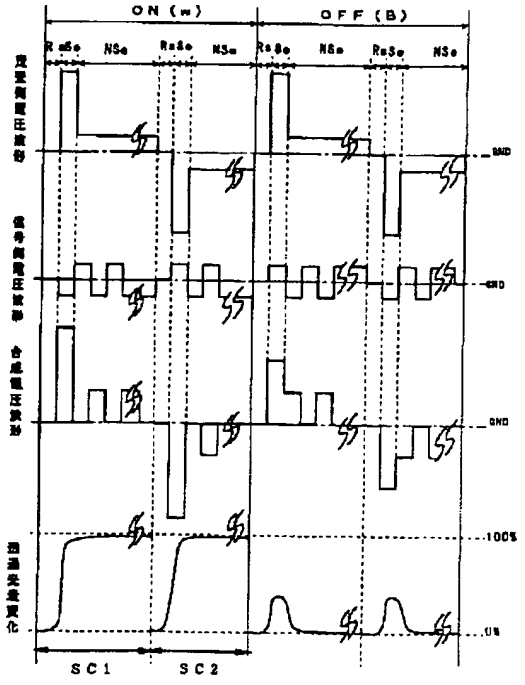
(54)【発明の名称】　反強誘電性液晶表示素子の駆動方法

(57)【要約】

【課題】　焼き付け現象を低減し、高速で高コントラストな表示を行うための反強誘電性液晶表示素子の駆動方法を提供する。

【解決手段】　リセット期間で反強誘電性液晶セル間の電位差を０Ｖにし、さらに走査側電極と信号側電極をグラウンドと短絡することでセル間および駆動回路での残留電荷成分を除去し、電荷量の差から起きる焼き付け現象を低減させる。



【特許請求の範囲】

【請求項１】　対向面にそれぞれ複数の走査側電極と信号側電極とを有する１対の基板間に反強誘電性液晶を挟持し、マトリックス状に画素を有する反強誘電性液晶表示素子の駆動方法であって、前記反強誘電性液晶は第１の強誘電状態と、第１の強誘電状態とは逆極性の電圧を印加した場合に強誘電状態を示す第２の強誘電状態と、反強誘電状態の３つの状態を有し、

画素への一回の書き込みは少なくとも一つの走査期間からなり、前記走査期間は画素の透過光量を決定するためのセレクトパルスが印加される選択期間と、この選択期間以前に、反強誘電性液晶を一定の状態にセットするリセットパルスを印加するリセット期間と、選択期間で決定した透過光量を保持する非選択期間とを有し、

前記リセット期間に於いて走査側電極と信号側電極は共にグラウンドと短絡することを特徴とする反強誘電性液晶の駆動方法。

【請求項２】　前後する走査期間の電圧波形が０Ｖに対して互いに対称であることを特徴とした請求項１記載の反強誘電性液晶表示素子の駆動方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、反強誘電性液晶を液晶層とする、マトリックス状の画素を有する液晶表示パネルや液晶光シャッターアレイ等の反強誘電性液晶表示素子の駆動法に関するものである。

【０００２】

【従来の技術】反強誘電性液晶を用いた液晶パネルは、日本電装（株）及び昭和シェル石油（株）らの特開平２－１７３７２４号公報で広視野角を有すること、高速応答が可能なこと、マルチプレックス特性が良好なこと等が報告されて以来、精力的に研究がなされている。

【０００３】図２は反強誘電性液晶をディスプレイとして用いる場合の偏光板配置を示す液晶セル構成図である。クロスニコルに合わせた偏光板２１の間に、どちらかの偏光板の偏光軸と無電界時に於ける分子の光軸方向がほぼ平行になるように液晶セル２２を置き、電圧無電界時に黒が、電界印加時には白が表示できるようにしている。このようなセル構成の液晶セルに電圧を印加したとき、それに対する透過率変化をグラフにプロットすると図３のようなループを描くことが出来る。電圧を印加し増加させていく場合に透過率が変化し始める電圧値をＶ１、透過率の変化が飽和する電圧値をＶ２、逆に電圧値を減少させていく場合に透過率が減少し始める電圧値をＶ５、また逆極性の電圧を印加し、その絶対値を増加させた場合に透過率が変化し始める電圧値をＶ３、透過率変化が飽和する電圧値をＶ４、逆に電圧の絶対値を減少させた場合に透過率が変化し始める電圧値をＶ６とする。この図３からは、電圧値が反強誘電性液晶分子の閾値以上をとる場合に第１の強誘電状態が選択され、また印加電圧の極性の違いによって、第２の強誘電状態が選択され、これらの強誘電状態から、電圧値がある閾値より低い場合には反強誘電状態が選択されることがわかる。

【０００４】従来の駆動方法に於いては、図４に示すように、選択期間（Ｓｅ）で第１、もしくは第２の強誘電状態、もしくは反強誘電状態を選択し、その状態を次の非選択期間（ＮＳｅ）で保持させていた。つまり選択期間（Ｓｅ）で印加したセレクトパルスによる透過光量をその後の非選択期間（ＮＳｅ）で保持させることにより表示を行っていた。

【０００５】また選択期間に印加されるセレクトパルスの直前で、反強誘電性液晶の分子状態が異なると、画素の透過光量を正確な所定の値にする事が難しく、そのためセレクトパルスを印加する前に、その画素の表示以前の状態に関わらず常に反強誘電状態にリセットすることが良く行われてきた。この反強誘電状態にリセットする方法としては、リセット期間内の電圧値を０Ｖにし、反強誘電性液晶自身の持つ粘性や弾性などの特性による自然緩和によって反強誘電状態にリセットする方法や、適切な逆極性を有する印加電圧を印加して反強誘電状態にリセットする方法がある。

【０００６】

【発明が解決しようとする課題】しかしながら前者の、反強誘電性液晶分子の強誘電状態からの自然緩和によるリセット法の場合には、確実に反強誘電状態にリセットすることができるが、リセット期間直前の画素の状態が第１または第２の強誘電状態の場合には、液晶層間の電荷に着目すると以前の書き込みによる電荷が全く残らない初期状態にするためには多くの時間が必要となり、画面の書き込み時間が遅くなってしまう。また後者の、適切な電圧を印加し反強誘電状態にリセットする方法の場合にも同様に、リセット期間直前の状態が第１の強誘電状態であれば－（マイナス）の極性の電圧を、第２の強誘電状態の場合には＋（プラス）の極性の電圧を印加するが、液晶層間には常に電圧が印加することになり、余計な電荷が存在する。このように従来のような反強誘電状態にリセットする方法では電荷の放電経路がないために以前の表示状態によって影響を受け、その結果表示画面が焼き付くという欠点があった。

【０００７】また、反強誘電状態にリセットする方法に類似した技術で、書き込み時に反強誘電性液晶を一度強誘電状態にする方法が特開平５－１００２０８に開示されている。

【０００８】特開平５－１００２０８の実施例では階調電圧を印加する前に強誘電状態に転移するのに充分な電圧を印加し、液晶の応答性（立ち上がり速度）を高めている。しかし、特開平５－１００２０８では反強誘電性液晶を強誘電状態にする速度の向上を目的とするもので、反強誘電状態へ転移させる駆動については触れられ

ていない。

【０００９】そこで本発明ではこれらの問題点を解決し、セル間および駆動回路での残留電荷成分の電荷量の差から起きる焼き付け現象を低減し、高速で高コントラストな表示を行うための反強誘電性液晶表示素子の駆動方法を提供することを目的としている。

【００１０】

【課題を解決するための手段】上記目的を達成するために本発明における反強誘性電液晶表示素子の駆動方法では、以下の手段を用いた。

【００１１】対向面にそれぞれ複数の走査側電極と信号側電極とを有する１対の基板間に反強誘電性液晶を挟持し、マトリックス状に画素を有する反強誘電性液晶表示素子で、前記反強誘電性液晶は第１の強誘電状態と、第１の強誘電状態とは逆極性の電圧を印加した場合に強誘電状態を示す第２の強誘電状態と、反強誘電状態とを有し、画素への一回の書き込みは少なくとも一つの走査期間からなり、走査期間は画素の透過光量を決定するためのセレクトパルスが印加される選択期間と、この選択期間以前に、反強誘電性液晶分子を一定の状態にセットするためのリセットパルスを印加するリセット期間と、選択期間で決定した透過光量を保持する非選択期間とから構成され、リセット期間に於いて走査側電極と信号側電極は共にグラウンドと短絡することを特徴とする。

【００１２】そして、画素へ印加される前後する走査期間の電圧波形が０Ｖに対して互いに対称とし、交流化を図っている。

【００１３】（作用）反強誘電性液晶は図３に示すように印加電圧の絶対値がある閾値電圧以上の場合に第１または第２の強誘電状態をとる。この時、図２に示すようなセル構成の場合に、本発明の駆動方法によるリセット期間では必ず反強誘電性液晶分子が反強誘電状態になるようにする。このために、リセット期間では反強誘電性液晶分子が第１または第２の強誘電状態から反強誘電状態にスイッチングするために必要な閾値電圧を印加する。通常この電圧値は、第１もしくは第２の強誘電状態から第２もしくは第１の強誘電状態にスイッチングするために必要な電圧値よりも小さい。この電圧値を０Ｖにし、と同時に走査側電極側、信号側電極共にグラウンドと短絡することで液晶セル間および駆動回路での残留電荷成分を除去する。この方法を用いると、従来の反強誘電状態にリセットするための電圧が不要になる。また、液晶本来の持つ特性による自然緩和によって反強誘電状態にリセットする方法に比べて非常に高速にリセットすることができる。

【００１４】本願発明による駆動方法は、反強誘電性液晶の状態を一回の書き込みごとに反強誘電状態にリセットすると同時に、液晶セル間および駆動回路での残留電荷成分を除去するので、書き込みごとの表示を安定させ、かつリセット期間の印加電圧を０Ｖで反強誘電性液晶を反強誘電状態にできるので、リセットパルスの印加電圧も不要となる。また短い選択期間で、表示状態（反強誘電性液晶の状態）を決定するので、強誘電状態または反強誘電状態のどちらの状態にでも良好に状態を転移させながら、高速な表示が可能であり、残留電荷成分による焼き付き現象が低減される。本発明は、この点に着目して完成されたものであり、以下実施の形態に基づいて説明する。

【００１５】

【発明の実施の形態】以下本発明の実施の形態を図面に基づいて詳細に説明する。図５は本実施の形態に用いた液晶パネル構成図である。本実施の形態で用いた液晶パネルは約２μの厚さの反強誘電性液晶層５６を持つ一対のガラス基板５３ａ、５３ｂから構成されている。ガラス基板の対向面には電極５４ａ、５４ｂが形成されており、その上に高分子配向膜５５ａ、５５ｂが塗布され、ラビング処理がなされている。さらに一方のガラス基板の外側に偏光板の偏光軸とラビング軸とが平行になるように第１の偏光板５１ａが設置されており、他方のガラス基板の外側には第１の偏光板５１ａの偏光軸と９０°異なるようにして第２の偏光板５１ｂが設置されている。

【００１６】また図６は走査側電極と信号側電極の配置を表した図である。走査側電極をそれぞれＸ１、Ｘ２、Ｘｎ等と示し、信号側電極はＹ１、Ｙ２、Ｙｍ等と示し、走査側電極は４８０本、信号側電極は６４０本とした。それぞれが交差する斜線部分が画素（Ａ１１、Ａｎｍ）である。

【００１７】図１は本発明の実施の形態の白表示（ＯＮ(Ｗ)）および黒表示（ＯＦＦ(Ｂ)）を行う場合の走査側電極（Ｘｎ）での走査側電圧波形、信号側電極（Ｙｍ）での信号側電圧波形、およびそれらが交差したところの画素（Ａｎｍ）での合成電圧波形、およびそれに応じた透過光量の変化を示した図である。本発明に用いた駆動波形ではリセット期間（Ｒｓ）を１位相、選択期間（Ｓｅ）を１位相とした。１位相のパルス幅は５０μｓに設定し、１回の書き込みは２つの走査期間（ＳＣ１、ＳＣ２）から構成した。非選択期間（ＮＳｅ）の時間は約４５ｍｓであり、走査側電極（Ｘｎ）波形には非選択期間（ＮＳｅ）に４Ｖの保持電圧を印加し、この極性はリセット期間（Ｒｓ）に印加される電圧と同極性とした。

【００１８】走査側電極（Ｘｎ）のセレクト期間（Ｓｓ）に印加されるパルスの波高値の最大絶対値は２０Ｖとし、信号側電極（Ｙｍ）に印加される最大絶対値は４Ｖとした。黒表示（ＯＦＦ(Ｂ)）を行うためには第１走査期間（ＳＣ１）の合成電圧波形（Ａｎｍ）では、０Ｖが１位相印加され（リセットパルス）、反強誘電性液晶は反強誘電状態を示し、透過光量はリセット期間では０％近くなったが、次の選択期間（Ｓｅ）で、[illegible]形として＋２４Ｖが１位相だけ印加されるため、ブロック

トパルス）、反強誘電性液晶は第１もしくは第２の強誘電状態になり、透過光量は１００％となり、白表示ＯＮ（Ｗ）をする。非選択期間（ＮＳｅ）では強誘電性液晶は反強誘電状態を保持している。リセット期間は観測者の視覚認識に必要な期間より十分短いため、表示は白と視覚認定される。

【００１９】また、黒表示ＯＦＦ（Ｂ）の場合には、同様にリセット期間（Ｒｓ）の合成電圧波形で、０Ｖが１位相印加され（リセットパルス）、反強誘電性液晶は反強誘電状態を示し、透過光量はリセット期間で０％近くなり、次の選択期間（Ｓｅ）で、合成電圧波形として＋１６Ｖが１位相だけ印加されるため（セレクトパルス）、反強誘電性液晶は第１もしくは第２の強誘電状態まで至らず、反強誘電状態が選択され、透過光量は０％近く、黒表示になる。非選択期間（ＮＳｅ）では反強誘電性液晶はリセット期間と同様にして反強誘電状態を保持する。リセット期間は観測者の視覚認識に必要な時間より十分短いため、表示は黒と視覚認定される。

【００２０】また１回の書き込みで２つの走査期間（ＳＣ１、ＳＣ２）を設け、それぞれの電圧波形の極性は０Ｖに対して互いに対称とし、交流化を図った。

【００２１】前記手法を講じることで、リセットパルスの印加電圧は０Ｖであるが反強誘電性液晶が反強誘電状態にリセットする時間は従来に比べて短くできた。また、このように黒および白の如何なる表示においても、選択期間に要する時間を短縮することができ、どのような表示画面の場合でも良好な表示を高速で行うことができた。

【００２２】本実施の形態では、走査側電極と信号側電極を複数有する駆動について示したが、例えば画素がスイッチング素子であるようなアクティブ素子を使用した駆動の場合でも、画素に印加される電圧波形が、本実施の形態のような合成電圧波形であれば充分に同じ効果が得られる。

【００２３】

【発明の効果】以上の実施の形態で述べたように、本発明の駆動方法を用いて、リセット期間に液晶セル間および駆動回路をグラウンドと短絡することで、反強誘電性液晶を反強誘電状態にリセットし、さらに第１もしくは第２の強誘電状態のときの残留電荷成分を除去し、さらに駆動回路においても電荷を放電することで常に初期状態から新規に液晶セルに書き込みを行うことができるので、連続駆動による焼き付け現象を低減し、さらにそのリセット期間が短いため、高速でコントラストの高い良好な表示を行うことができる。

【図面の簡単な説明】

【図１】本発明の実施の形態における反強誘電性液晶表示素子の駆動波形とそれに対応する透過光量を示した図である。

【図２】本発明の実施の形態における反強誘電性液晶セルと偏光板の構成図である。

【図３】本発明の実施の形態における反強誘電性液晶表示素子のヒステリシスカーブを表す図である。

【図４】従来技術における反強誘電性液晶表示素子の駆動方法を示す図である。

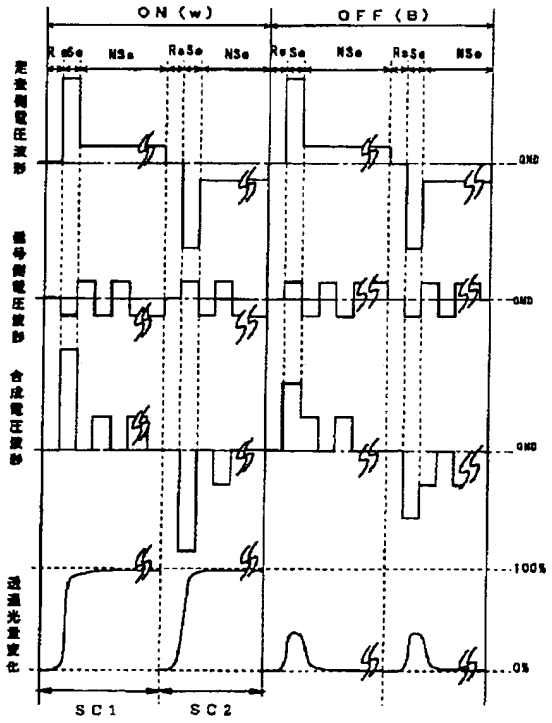
【図５】本発明の実施の形態における反強誘電性液晶パネルの構成図である。

【図６】本発明で実施の形態における走査側電極と信号側電極の構成図である。

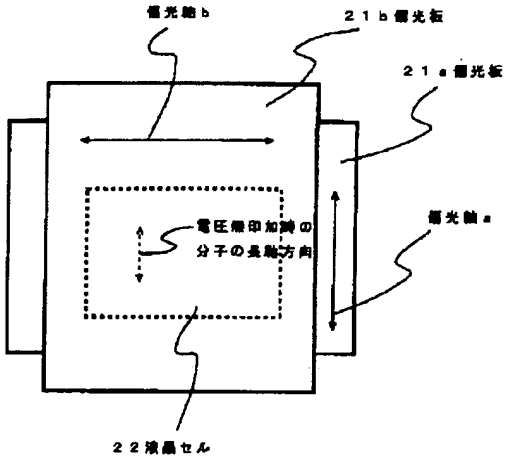
【符号の説明】

ＯＦＦ（Ｂ）　黒表示
ＯＮ（Ｗ）　白表示
ＳＣ１　第１走査期間
ＳＣ２　第２走査期間
Ｒｓ　リセット期間
Ｓｅ　選択期間
ＮＳｅ　非選択期間
Ｘｎ　走査側電極
Ｙｍ　信号側電極
Ａｎｍ　画素
Ｔ　透過光量
２１ａ、２１ｂ　偏光板
２２　液晶セル
５１ａ、５１ｂ　偏光板
５２ａ、５２ｂ　シール材
５３ａ、５３ｂ　ガラス基板
５４ａ、５４ｂ　電極
５５ａ、５５ｂ　高分子配向膜
５６　反強誘電性液晶
Ｘ１～Ｘ４８０　走査側電極
Ｙ１～Ｙ６４０　信号側電極
Ａ１１、Ａｎｍ　画素

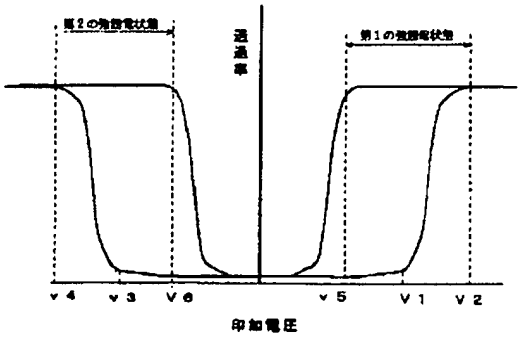
【図1】


ON (w)
OFF (B)
GND
100%
0%
SC1
SC2

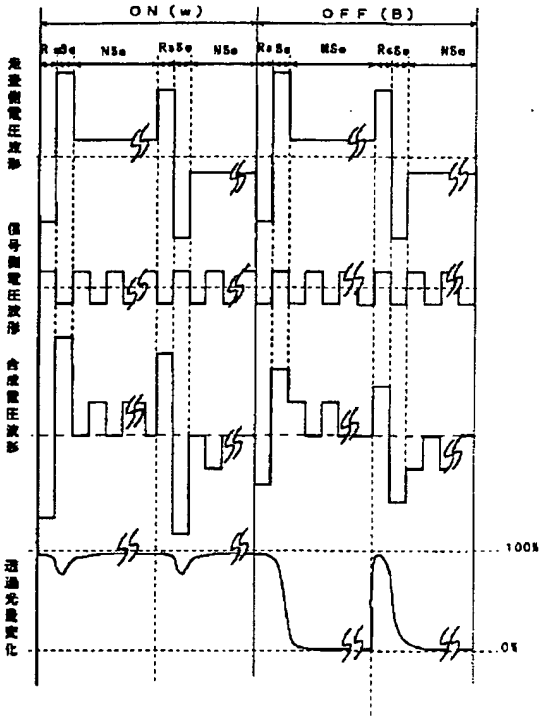
【図2】


偏光軸b
21b偏光板
21a偏光板
偏光軸a
電圧無印加時の
分子の長軸方向
22液晶セル

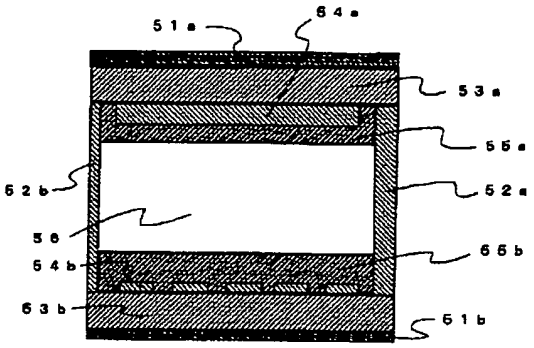
【図3】


透過率
印加電圧
V4
V3
V6
V5
V1
V2

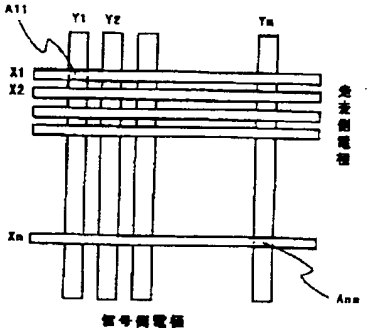
【図4】


ON (w)
OFF (B)
100%
0%

【図5】


51a
54a
53a
55a
52b
52a
56
54b
55b
53b
51b

【図6】


A11
Y1
Y2
Ym
X1
X2
走査側電極
Xn
Anm
信号側電極